

What is claimed is:

1 1. A memory array for a DRAM chip with open bit-line
2 architecture, comprising:
3 a plurality of gate-lines, each gate-line having a loop
4 portion with a first segment and a second segment;
5 and
6 a plurality of DRAM cells associated with each gate-line
7 and having first DRAM cells and second DRAM cells,
8 wherein the first DRAM cells have first gates
9 consisting of the first segment and the second DRAM
10 cells have second gates consisting of the second
11 segment; and
12 a plurality of bit-lines connected with the DRAM
13 cells, each of the bit-lines is connected to either
14 one of the first DRAM cells or one of the second DRAM
15 cells.

1 2. The memory array as claimed in claim 1, wherein the
2 gate-lines are defined and formed by using an alternating
3 phase-shift mask in conjunction with a single exposure process.

1 3. The memory array as claimed in claim 1, wherein the first
2 and the second DRAM cell have active areas defined by a dark loop
3 on a mask.

1 4. The memory array as claimed in claim 3, wherein the mask
2 is an alternating phase-shift mask and, during a lithography
3 process, first light traversing a first portion enclosed by the
4 dark loop and second light traversing a second portion adjacent
5 the dark loop are 180 out of phase.

1 5. A alternating phase-shift mask for defining gate
2 patterns on a DRAM chip with open bit-line
3 architecture, comprising:
4 opaque lines for defining gate-lines of a memory array in
5 the DRAM chip, each opaque line having:
6 a dark loop;
7 a first portion enclosed and defined by the dark loop;
8 and
9 a second portion adjacent the dark loop;
10 wherein, during a lithography process, first light
11 traversing the first portion and second light
12 traversing the second portion are 180 out of
13 phase.

1 6. A alternating phase shift mask for defining active
2 areas on a DRAM chip, comprising:
3 opaque lines for defining active areas of a memory
4 array in the DRAM chip, each opaque line having:
5 a dark loop;
6 a first portion enclosed and defined by the dark loop;
7 and
8 a second portion adjacent the dark loop;
9 wherein, during a lithography process, first light
10 traversing the first portion and second light
11 traversing the second portion are 180 out of
12 phase.

1 7. A memory array for a DRAM chip, comprising:
2 a plurality of DRAM cells, arranged in rows and columns,
3 wherein a first edging DRAM cell at one end of a first

4 row has a common active area shared with a second
5 edging DRAM cell at one end of an adjacent row, the
6 common active area is defined by a dark loop on an
7 alternating phase-shift mask, and, during a
8 lithography process, first light traversing a first
9 portion enclosed by the dark loop portion and second
10 light traversing a second portion adjacent the dark
11 loop portion are 180 out of phase.

1 8. The memory array as claimed in the claim 7, further
2 comprising:
3 a plurality of gate-lines, each gate-line having:
4 a loop portion with a first segment and a second
5 segment; and
6 a plurality of bit-lines connected with the DRAM
7 cells;
8 wherein the plurality of DRAM cells have first DRAM cells
9 and second DRAM cells, the first DRAM cells have first
10 gates consisting of the first segment, the second DRAM
11 cells have second gates consisting of the second
12 segment, and each of the bit-lines is connected to
13 either one of the first DRAM cells or one of the second
14 DRAM cells to construct open bit-line structure.

1 9. A method for manufacturing DRAM chips, comprising:
2 providing a first alternating phase-shift mask, having:
3 opaque lines, each opaque line having a dark loop;
4 a first portion enclosed and defined by the dark loop;
5 and
6 a second portion adjacent the dark loop, wherein,
7 during a lithography process, first light

8 traversing the first portion and second light
9 traversing the second portion are 180 out of
10 phase;
11 patterning, through the lithography process in together
12 with the first alternating phase-shift mask, active
13 areas of a memory array, wherein at least two edging
14 DRAM cells in the memory array share a common active
15 area.

1 10. A method for manufacturing DRAM chips, comprising:
2 providing a first alternating phase-shft mask, having:
3 opaque lines, each opaque line having a dark loop;
4 a first portion enclosed and defined by the dark loop;
5 and
6 a second portion adjacent the dark loop, wherein,
7 during a lithography process, first light
8 traversing the first portion and second light
9 traversing the second portion are 180 out of
10 phase;
11 patterning, through the lithography process in together
12 with the first alternating phase-shift
13 mask, gate-lines of a memory array, wherein each
14 gate-line has a loop portion corresponds to the dark
15 loop on the first alternating phase-shft mask.